

DDR4 SODIMM Slot Compliance Interposer

Flexible Command Timing Compliance Validation

- Cost Optimized Visibility
- Address, Command and Control Timing with Command Decode
- Passive 260-pin DIMM Slot Interposer
- Designed for Speeds of DDR4 2400+ *
- Automated Logic Analyzer Setup for fast Time-to-Data
- DDR4 Compliance Analysis S/W (optional)
- Compatible with Nexus Memory Analyzer (MA) Instrument

* The Tektronix LA supports State, MagniVu and iCapture up to 2800+. The MCA4000 cross-triggering enables supports MagniVu and iCapture up to 3000+.

Overview

Nexus Technology recommends DDR4 slot interposers for applications where the customer must have the greatest flexibility for probing of different DDR4 DIMMs.

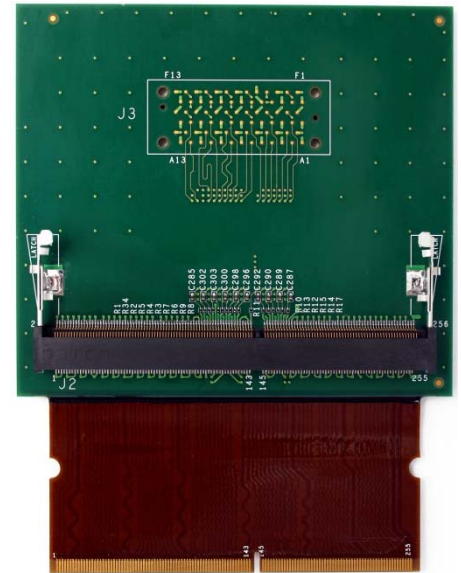
This interposer is an extender design and does not require a dedicated SODIMM slot. The flex design provides mechanical clearance around the SODIMM Slot.

This is a passive interposer with no added buffers to conceal system performance.

Performance You Can See™



Figure 1 - State Display of Command, Address & Control



The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides disassembly of the DDR4 transactions (Command, Address and Control only) for easy display of the DDR bus cycles and logic analyzer settings for triggers and filters.

Logic analyzer setup software (TLA support package) included with this product acquires/reconstructs the command/address bus. The software also decodes and displays the bus command sequence and provides easy DDR command sequence triggering to quickly capture relevant commands.



iCapture Analog Mux

The logic analyzer also comes standard with iCapture Analog Mux. This provides the ability to see *any* channel of the DDR bus in seconds on an oscilloscope. This is invaluable information which allows analysis within minutes as to the status and behavior of the DDR4 bus. No extra probing is required to gain analog incite of the DDR4 bus. This information can be pushed back into the logic analyzer software and viewed in a waveform window along with the state or timing data using the iView feature.

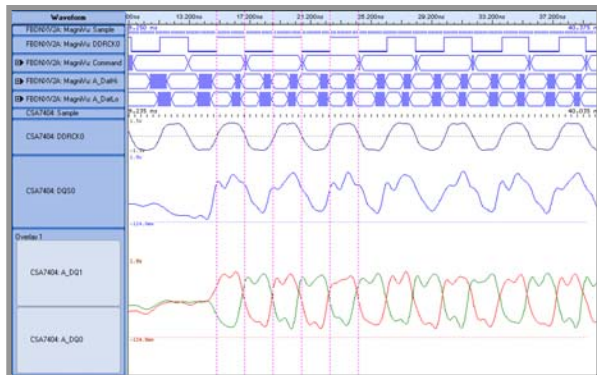


Figure 4 Example Representation of iView

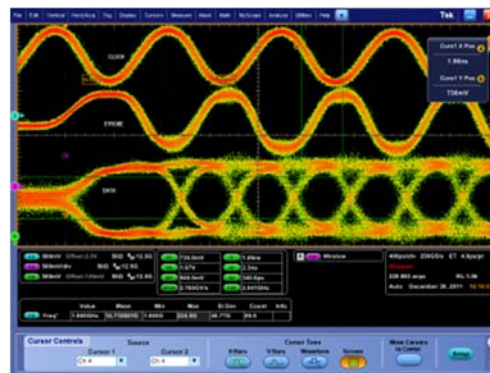


Figure 5 iCapture Analog Mux

Taking advantage of the ultra-high fidelity “Scope Probe per Signal” capability of the DDR4DIMM Interposer, iCapture enables focused analog level analysis and validation.

Compliance Analysis Software

The optional DDR4 Memory Compliance Analysis package enables and automates measurement of the DDR4 bus activity for fast and easy functional testing and extensive compliance, statistical, and performance analysis.

- Extensive JEDEC DDR4 Compliance Analysis
- Quick and Easy Setup w/No Calibration Required
- Automated Acquisition and Measurement
- Powerful in-application graphical and tabular analysis results
- Memory controller & JEDEC parameters predefined
- Quickly navigate through multiple acquisitions
- Listing & waveform windows with violation analysis built in

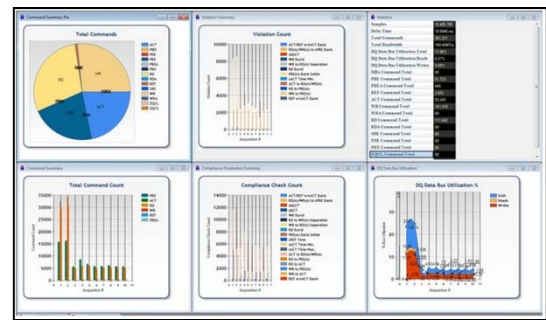


Figure 6

	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec.
R1 R0	NA	NA	NA	NA	959,880
R2 R1 R0	28,007	10,273,985	2,106,353	6.7	26,250
R3 R2 R1 R0	7,441	878,808	123,227	3.3	7,200
R4 R3 R2 R1 R0	NA	NA	NA	NA	5,625
R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	70,200,000
R6 R5 R4 R3 R2 R1 R0	1,855	8,189,726	945,496	-85.9	13,125
R7 R6 R5 R4 R3 R2 R1 R0	114,121	8,169,101	6,001,631	3.7	110,000
R8 R7 R6 R5 R4 R3 R2 R1 R0	42,969	2,839,180	267,945	14.6	37,500
R9 R8 R7 R6 R5 R4 R3 R2 R1 R0	42,969	2,839,180	267,945	-99.9	70,200,000
R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0	18,652	116,172	20,254	42.1	13,125
R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0	13,066	316,308	170,537	16.1	11,250
R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0	NA	NA	NA	NA	20,625
R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 R0	37,383	326,054	162,946	10.8	33,750

Figure 7 Tabular Results Detail of Compliance Analysis

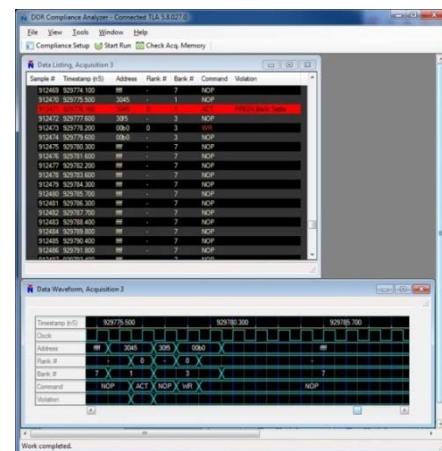


Figure 8 Waveform & Timing Displays of Compliance Analysis

Item	Item Name	Occurrences	Violations	Items	Min(ps)	Max(ps)	Average(ps)	Margin(%)	Spec. Value	Description
1	ACT to PRE Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
2	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
3	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
4	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
5	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
6	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
7	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
8	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
9	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
10	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
11	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
12	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
13	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
14	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
15	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
16	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
17	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
18	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
19	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
20	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
21	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
22	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
23	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
24	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
25	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
26	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
27	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
28	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
29	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
30	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
31	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
32	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
33	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
34	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
35	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
36	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
37	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
38	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
39	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.
40	PRE to ACT Delay	0	0	0	NA	NA	NA	NA	NA	Sequential check. A full Refresh Cycle (PRE) command cannot occur as a self-refreshing cycle.

Figure 9

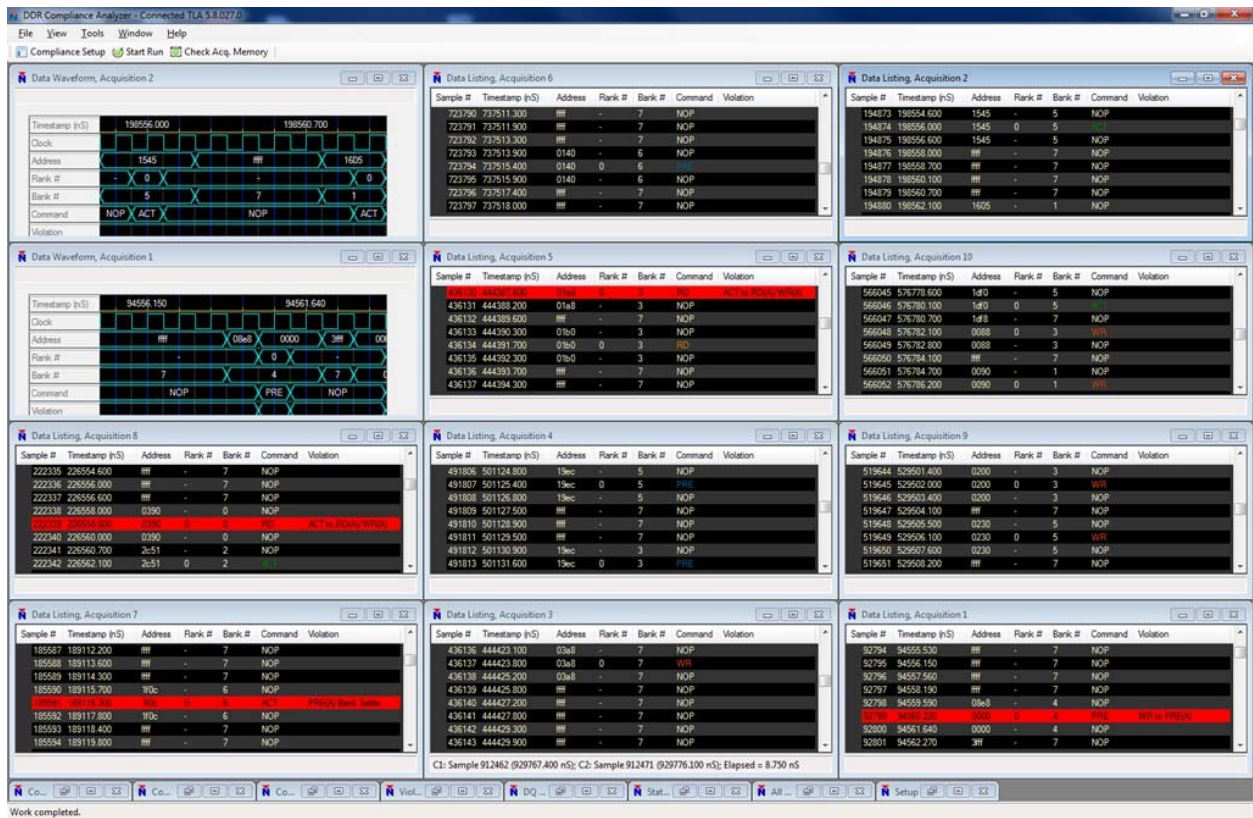


Figure 10 View of Violation in Data Across Many Acquisitions

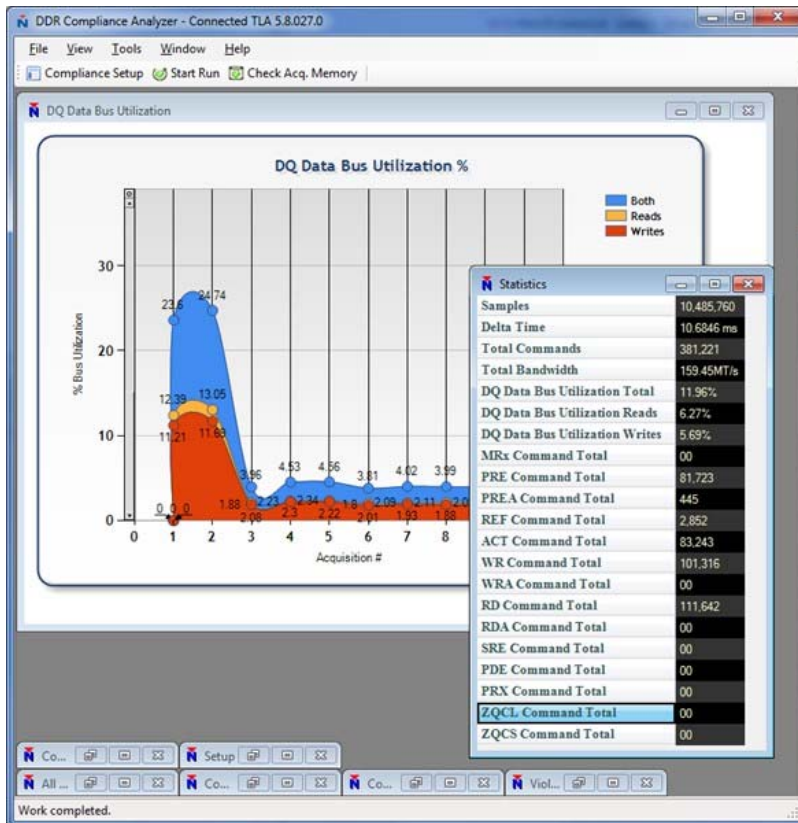


Figure 11 Bus Utilization Measurements

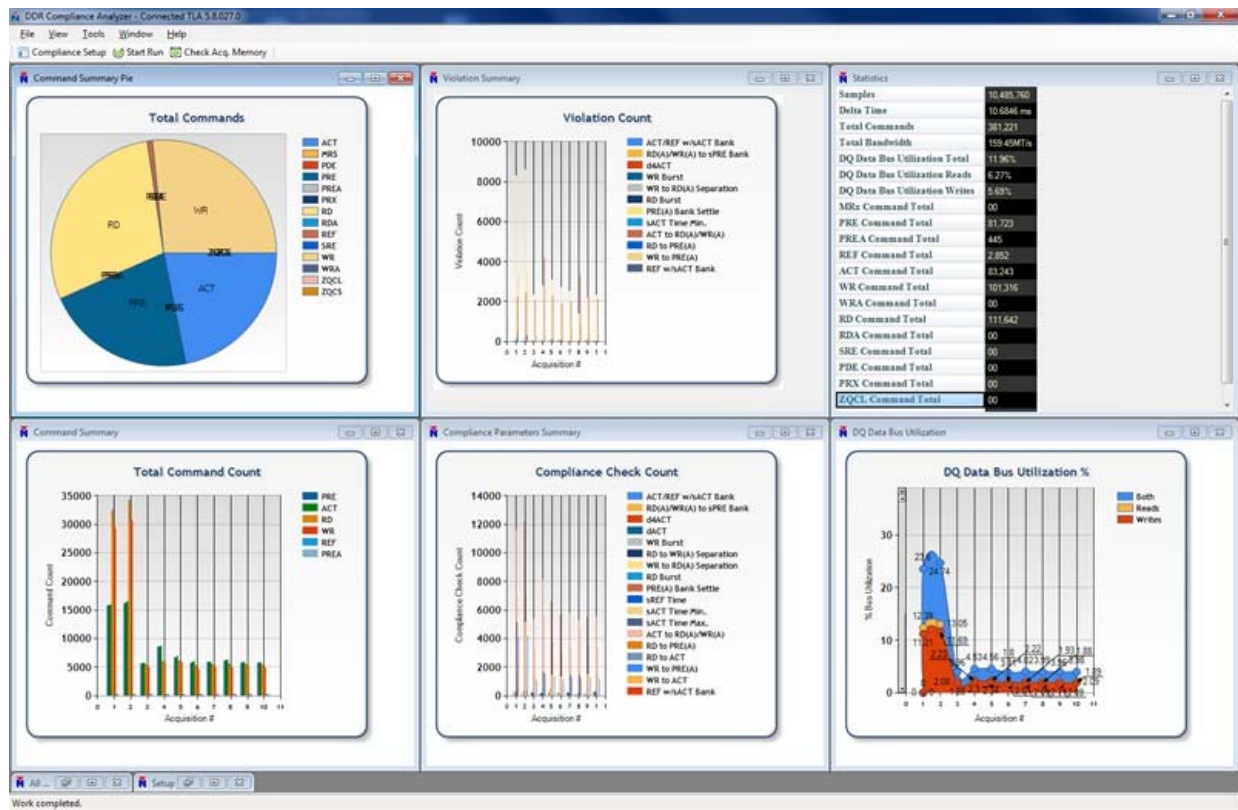


Figure 12 Graphical and Tabular Compliance Analysis Example

DDR System Setup

System Name: DDR3-1600

DDR System: DDR3-1600

DDR Spec: 800 MHz DDR Clock

of Ranks (Chip Selects): 4

Total Addressable Space: 512 Mb

Data bus (DQ): x 8

Addressing Length: 8

High Temp. Env. (85C-95C): ☐

CKE Mapping: ☐

Read/Writes:

- Additive Latency: 0
- Additive Latency Reserved (AL): 10
- CAS Latency (CL): 11
- CAS Write Latency (CWL): 8
- Burst Length: 8-bit
- Write Recovery (WR): 12
- Registered: ☐

Information:

- # of Banks: 8
- Rank Memory (64-bit): 536 MB
- System Memory (64-bit): 2144 MB
- Page Size: 1 KB
- Read Latency (RL): 11
- Write Latency (WL): 8
- Row Address Length (bits): 13
- Column Address Length (bits): 10
- WRA Precharge Delay: 24
- Min. RDA Precharge Delay: 4

Setup is valid

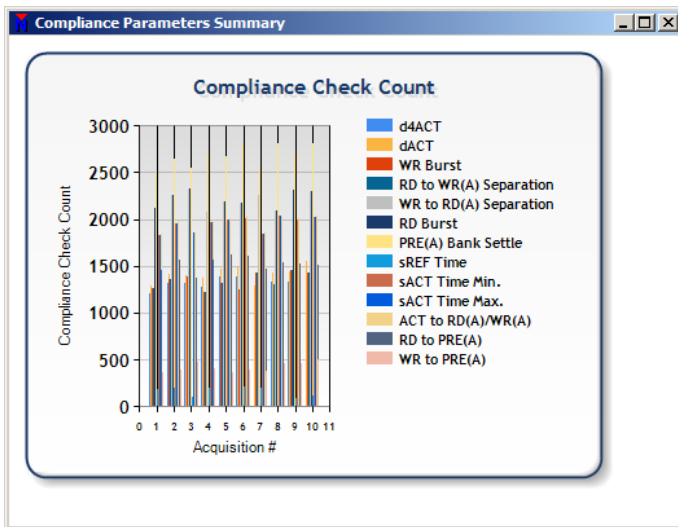
Save

Compliance Timing Parameters

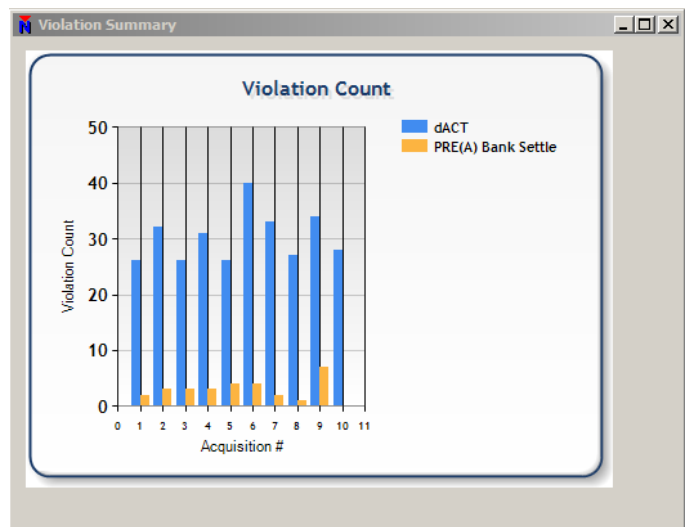
Timing Parameters: DDR3-800D

Parameter	Value	Unit	Parameter	Value	Unit
tACTPDEN	1	ck	tRASmin	37500	ps
tCCD	4	ck	tRCD	12500	ps
tCKESR	10	ns	tRDPDEN	Derived	ck
tDLLK	512	ck	tREFPDEN	1	ck
tFAW_1kb	40	ns	tRFC_512Mb	90	ns
tFAW_2kb	50	ns	tRFC_1Gb	110	ns
tMOD	12	ck	tRFC_2Gb	160	ns
tMRD	4	ck	tRFC_4Gb	300	ns
tMRSPDEN	12	ck	tRFC_8Gb	350	ns
tPDmin	7500	ps	tRP	12500	ps
tPDmax	70200	ns	tRRD_1kb	10	ns
tPDmax_HT	35100	ns	tRRD_2kb	10	ns
tPREPDEN	1	ck	tRTP	7500	ps
tRASmax	70200	ns	tWR	15	ns
tRASmax_HT	35100	ns	tWRPDEN	Derived	ck

Save



Shows the distribution of commands that were compliance checked



Shows the distribution of commands that violated the spec

DDR4 SODIMM Slot Compliance Interposer

NEX-SODDR4INTR-CMPL Technical Specification

General

Specification	Detail
Interface Type	Passive Interposer
LA Interface	NEX-PRB1XL
JEDEC Module Type	DDR4 SDRAM Unbuffered SODIMM
DDR4 Data Rates Supported (MT/s)	DDR4-2400+
Min. Voltage Swing	200mv
Min. Eye Width	200ps

Tektronix Hardware

Specification	Detail	Quantity
Logic Analyzer Mainframe	TLA7000	1
Logic Analyzer Module(s)	TLA7BB2/3/4 (1.4GHz Opt. Required)	1
Logic Analyzer Probes	NEX-PRB1XL	1

Nexus Memory Analyzer Configurations

Nomenclature	Detail
NEX-MA4150-DDR4	Memory Analyzer with DDR4 performance, margins and capture up to DDR4-3200 (1.6GHz) with 1G-Sample acquisition depth, ClockSafe™ and Single Smart Frequency Analysis. Additional Support for DDR3 Available as an option. Requires: Qty 1 NEX-PRB1XL
NEX-MA4120-DDR4	Memory Analyzer: Logic analyzer capture only up to DDR4-3200 (1.6GHz) with 512M-Sample acquisition depth. Options available for 1G-Sample, performance, margins, ClockSafe™ and Single Smart Frequency Analysis. Options also available to add DDR3 support. Requires: Qty 1 NEX-PRB1XL
NEX-MA4100-DDR4	Entry level Memory Analyzer with DDR4 performance, margins and capture up to DDR4-2667 (1.34GHz) with 512M-Sample Acquisition depth. Options include 1G-Sample, Clocksafe™, and Single Smart Frequency Analysis. Options also available to add DDR3 Support. Requires: Qty 1 NEX-PRB1XL

Product Configurations

Nomenclature	Detail
NEX-SO4INTR260-CMPL	1 – DDR4 260 pin SODIMM Address, Command, Control Interposer
NEX-MCATLA-DDR4-SWL	1 – DDR4 Compliance Analysis Software License (Optional)

Further Information

Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EDT/EST.

Web	www.nexustechnology.com
Telephone	877.595.8116
International	603.329.3083
Fax	877.595.8118
Address	78 Northeastern Blvd. Unit 2 Nashua, NH 03062
Email	support@nexustechnology.com

