MA4100 Memory Analyzer

Benchtop Memory Analyzer

Specifications

- DDR4-3200
- DDR3-3200
- ClockSafe™
- 1G-sample acquisition depth
- Programmable probe termination
- 11ps x 10mV x 20-channel analog characterization (iCiS™)
- Real-time analysis
- Real-time memory performance metrics
- Real-time memory compliance margins and validation
- Trigger in and trigger out

Key Features

- Application software ready for bench, remote-to-lab or offline operation
- Application includes advanced listing, waveform, tables and charting
- Turnkey setup, including automated MRS capture and analysis
- Patented interposer/probe designs
- Analyze thousands of real-time memory parameters
- Full featured, industry standard trigger system
- Automated analysis runs for everything from detailed setup information to quick summary runs, to in-depth extended data logging or margin testing runs
- ClockSafe™: Continuous analysis across clock stops and clock frequency changes
- Analog eye characterization on 20-channels simultaneously at 11ps x 10mV
- Correlate with an oscilloscope for memory DQ data capture
- Integrated Windows 10 Controller

Applications

- DDR4 and/or DDR3
- Memory validation and debug
- Monitoring bus traffic
- Bus traffic measurement
- Optimization of memory performance
- Analog insight
- JEDEC JESD79-4 rates to DDR4-3200
- JEDEC JESD79-3 rates to DDR3-3200

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Results Overview

State Capture

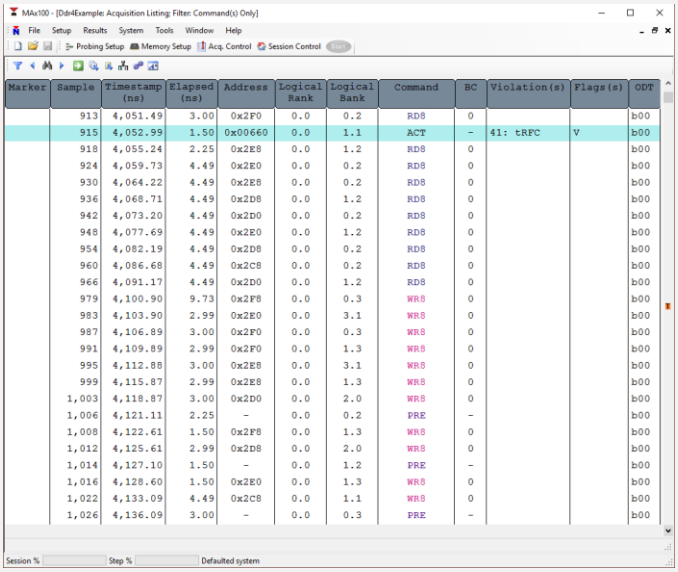


Figure 1 DDR4 State Listing Example

State capture results include continuous traffic around one or more events of interest. The traffic, which may consist of time, bus commands, bus addressing, margin violations, and trigger events, is presented in listing or waveform displays.

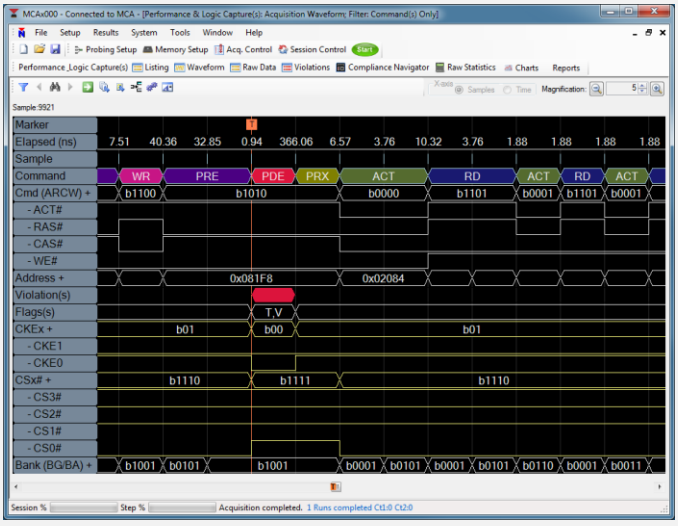


Figure 2 DDR4 Waveform Example

State capture depths from one hundred samples to one billion samples is available. Advanced acquisition controls monitor and respond to the continuous traffic in real-time to best utilize the state capture memory. Advanced post-capture search and filter can quickly parse the acquisition store.

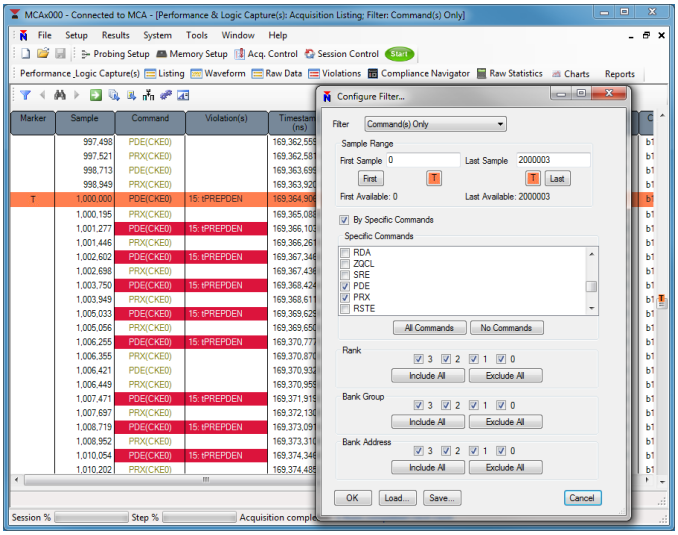


Figure 3 DDR4 Listing Filter/Search Example

Real-time Continuous Analysis

Real-time analysis provides data results during and after analysis runs which may be extremely long (days) or very short (nano-seconds). During the run, analysis is continuous and in real-time. Any event that occurs during the run is captured and analyzed.

Performance

Memory performance metrics include real-time margin metrics and margin violations. For each margin test, results indicate test coverage, observed margin values, as well as flags indicating margin violations. All data is continuously acquired in real-time with results updates continuously while the analyzer is still running. Memory performance metrics also include continuous real-time charting of bus performance characteristics such as throughput, utilization, power management, and more.

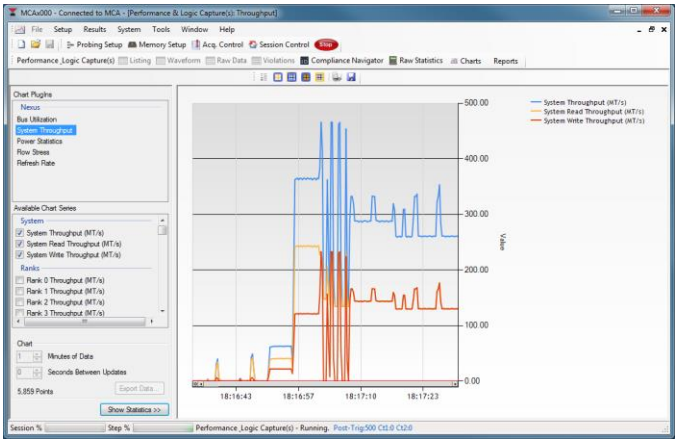


Figure 4 DDR4 Real-time / Performance Results Example

True Analog Visibility

iCiS™ provides detailed and invaluable insight of signal quality and expected performance for data acquisition you can trust.

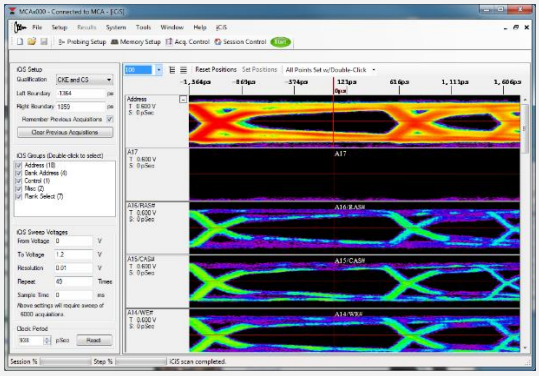


Figure 5 DDR4 iCiS™ Example

Automated Analysis

Analysis is automated and continuous from the time the user clicks the Start button until the analysis session completes. While running, the session updates the application with real-time results.

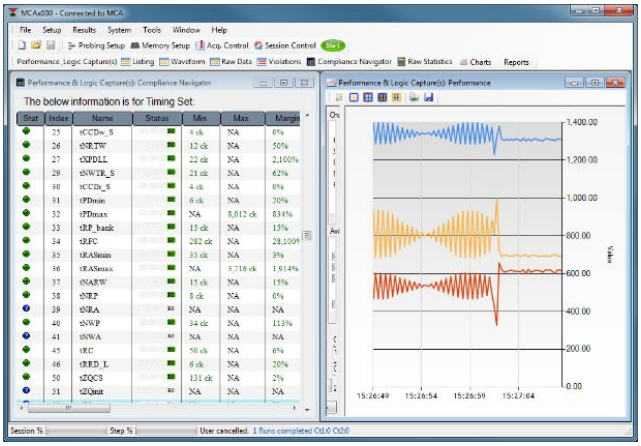
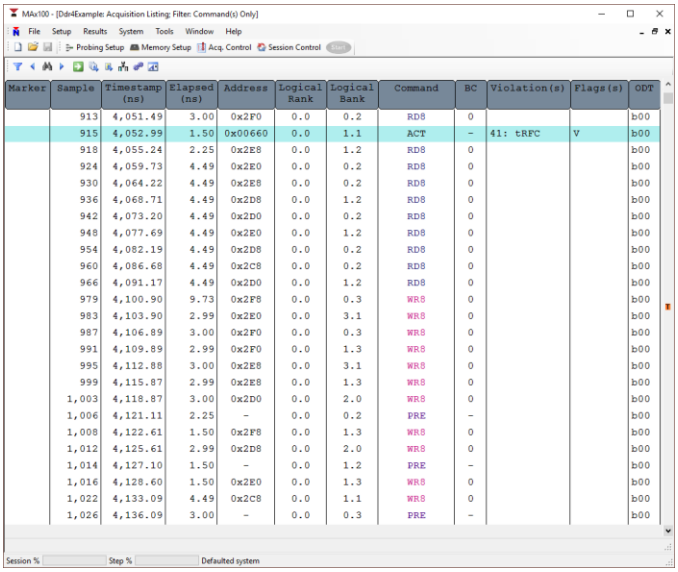


Figure 6 MA5100 Performance Metrics

In the MA5100 Performance Metrics image you can see real-time margins for all compliance parameters as well as a chart of read/write bus throughput.



Marker	Sample	Timestamp (ns)	Elapsed (ns)	Address	Logical Rank	Logical Bank	Command	BC	Violation(s)	Flags(s)	ODT
	913	4,051.49	3.00	0x2F0	0.0	0.2	RD8	0			b00
	915	4,052.99	1.50	0x00660	0.0	1.1	ACT	-	41: tRFC	V	b00
	918	4,055.24	2.25	0x2E8	0.0	1.2	RD8	0			b00
	924	4,059.73	4.49	0x2E0	0.0	0.2	RD8	0			b00
	930	4,064.22	4.49	0x2E8	0.0	0.2	RD8	0			b00
	936	4,068.71	4.49	0x2D8	0.0	1.2	RD8	0			b00
	942	4,073.20	4.49	0x2D0	0.0	0.2	RD8	0			b00
	948	4,077.69	4.49	0x2E0	0.0	1.2	RD8	0			b00
	954	4,082.19	4.49	0x2D8	0.0	0.2	RD8	0			b00
	960	4,086.68	4.49	0x2C8	0.0	0.2	RD8	0			b00
	966	4,091.17	4.49	0x2D0	0.0	1.2	RD8	0			b00
	979	4,100.90	9.73	0x2F8	0.0	0.3	WR8	0			b00
	983	4,103.90	2.99	0x2E0	0.0	3.1	WR8	0			b00
	987	4,106.89	3.00	0x2F0	0.0	0.3	WR8	0			b00
	991	4,109.89	2.99	0x2F0	0.0	1.3	WR8	0			b00
	995	4,112.88	3.00	0x2E8	0.0	3.1	WR8	0			b00
	999	4,115.87	2.99	0x2E8	0.0	1.3	WR8	0			b00
	1,003	4,118.87	3.00	0x2D0	0.0	2.0	WR8	0			b00
	1,006	4,121.11	2.25	-	0.0	0.2	PRE	-			b00
	1,008	4,122.61	1.50	0x2F8	0.0	1.3	WR8	0			b00
	1,012	4,125.61	2.99	0x2D8	0.0	2.0	WR8	0			b00
	1,014	4,127.10	1.50	-	0.0	1.2	PRE	-			b00
	1,016	4,128.60	1.50	0x2E0	0.0	1.3	WR8	0			b00
	1,022	4,133.09	4.49	0x2C8	0.0	1.1	WR8	0			b00
	1,026	4,136.09	3.00	-	0.0	0.3	PRE	-			b00

Figure 7 Violation on Line 915

In this example, the analyzer is configured to continuously monitor acquire data until the first occurrence of a compliance violation occurs. That's three simultaneous measurements, each collecting/monitoring real-time data.

ClockSafe™

The memory clock stops and changes frequencies during initialization and calibration. It may also stop and change frequencies during normal operation. ClockSafe™ provides continuous acquisition across these clock stops and frequency changes through a robust acquisition interface that can handle any clock frequency from 0MHz to 1.6GHz.

Reliable Connection

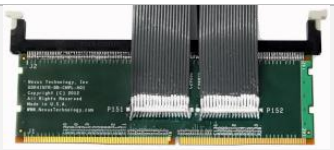
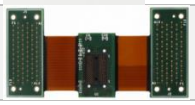
DDR4 and DDR3 interposers and probes provide connection between the analyzer and the target while preserving analog signal characteristics.

Attachment Service

Memory component BGAs typically live on densely populated targets. This presents a challenging probing environment and an opportunity to provide our expert services. We provide attachment services for all our component/package interposers so that our customers are up and running quickly and reliably.

Figure 8 Attachment Service Example

MA5100 Analyzer Interposers

Product Name	Specification	Type	Sockets / Risers Available	Product Image
DDR4-D-DIM-288	DDR4	DIMM Slot Interposer (UDIMM / RDIMM / LRDIMM)	NA	
DDR4-D-DIM-260	DDR4	SODIMM Slot Interposer	NA	
DDR4-D-CTS-78	DDR4	x4/x8 BGA Interposer	Yes	
DDR4-D-CTS-96	DDR4	X16 BGA Interposer	Yes	
DDR3-D-DIM-240	DDR3	DIMM Slot Interposer (UDIMM / RDIMM)	NA	
DDR3-D-DIM-204	DDR3	SODIMM	NA	
DDR3-D-CTS-78	DDR3	x4/x8 BGA Interposer	Yes	
DDR3-D-CTS-96	DDR3	x16 BGA Interposer	Yes	

* Custom interposers are always available

Analyzer Probes

Product Name	DDR Channels Supported	Channels Probed	Connection	DDR5	LPDDR5	DDR4	LPDDR4	DDR3	LPDDR3
PRB-HD-H10	1	1 diff.clock 10 channels	HD, Horiz.	x	x		x		X
PRB-HD-H20	1	1 diff. clock 20 channels	HD, Horiz.	x	x		x		X
PRB-HD-V10	1	1 diff. clock 10 channels	HD, Vert.	x	x		x		X
PRB-FL-20	1 or 2	1 diff. clock 20 channels	Flying-Lead	x	x	x	x	x	X
PRB-P69	1 or 2	1 diff. clock 32 channels	P6900 Midbus	x	x	x	x	x	x
PRB-XL-1	1 or 2	1 diff. clock 33 channels	DIMM / SOIMM	x	x	x	x	x	x

Product Configuration Table

Product Name	Description	Nexus Order Number
MA4100	Benchtop analyzer for DDR4 and DDR3.	Contact us for configuration options

SCAN ME

Figure 9 MA4100 Website

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