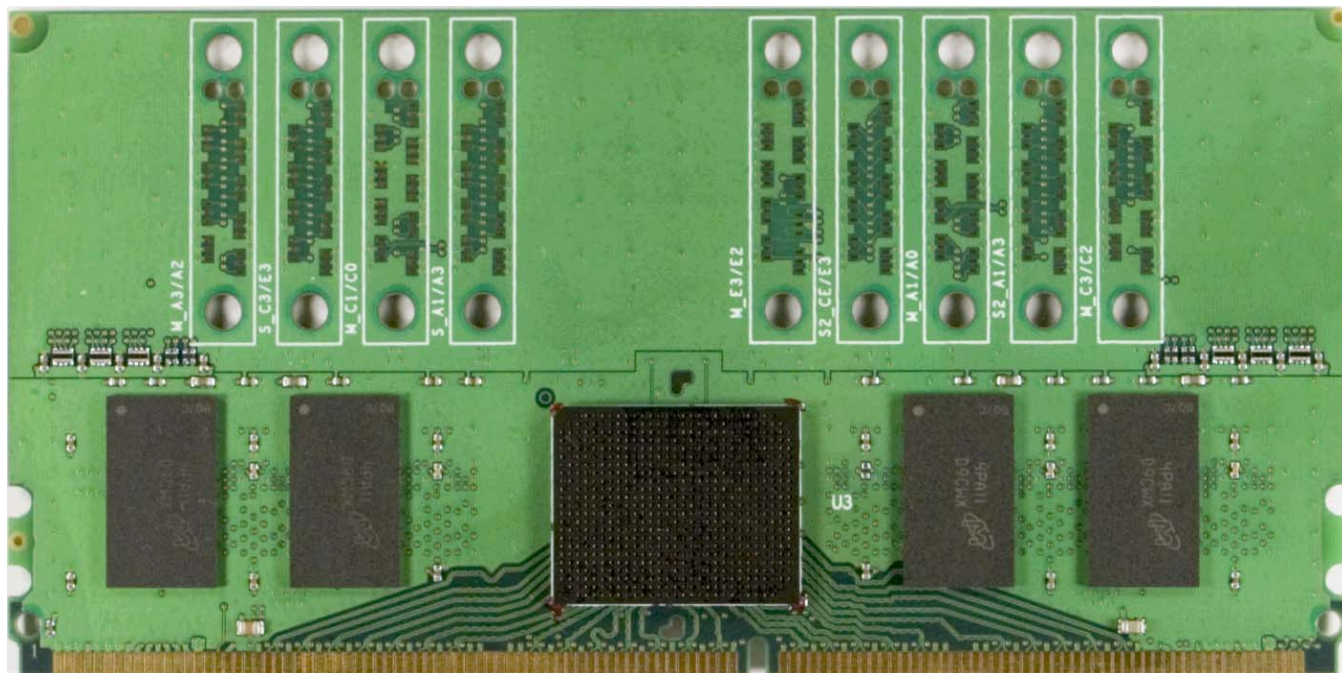


NEX-FBDNEXVu667x8DRx/x4SRx



- NEX-FBDNEXVu667x8DRx/4xSRx DIMM is designed to JEDEC FB DIMM standards with built-in TLA connections
- Innovative approach provides visibility of actual data as seen by the memory chips
- Micron Technology Memory Chips included on each DIMM
- FBD-NEXVu-x DIMMs without memory chips are available for use with alternate vendor memories
- Support for a variety of FB DIMM configurations (inquire for the latest configuration list)
- Acquisition of DDRII Address / Command, Read and Write data
- No logic analyzer interposer card to worry about impairing system performance at up to 800Mt/s data rates
- FB DIMM design does not require a dedicated slot
- Selective Clocking - filters Refresh & Idle Cycles for improved TLA memory utilization
- FB DIMMs have probe footprints on both sides of DIMM to permit probing from either side
- Accurate 8GHz timing analysis on every channel
- Time correlation with data from other acquisition modules

General Description

8GHz Timing Analysis available for all DDRII signals.

Oscilloscope Connectivity on any channel without re-probing via the TLA's Enhanced iView Analog Mux capability

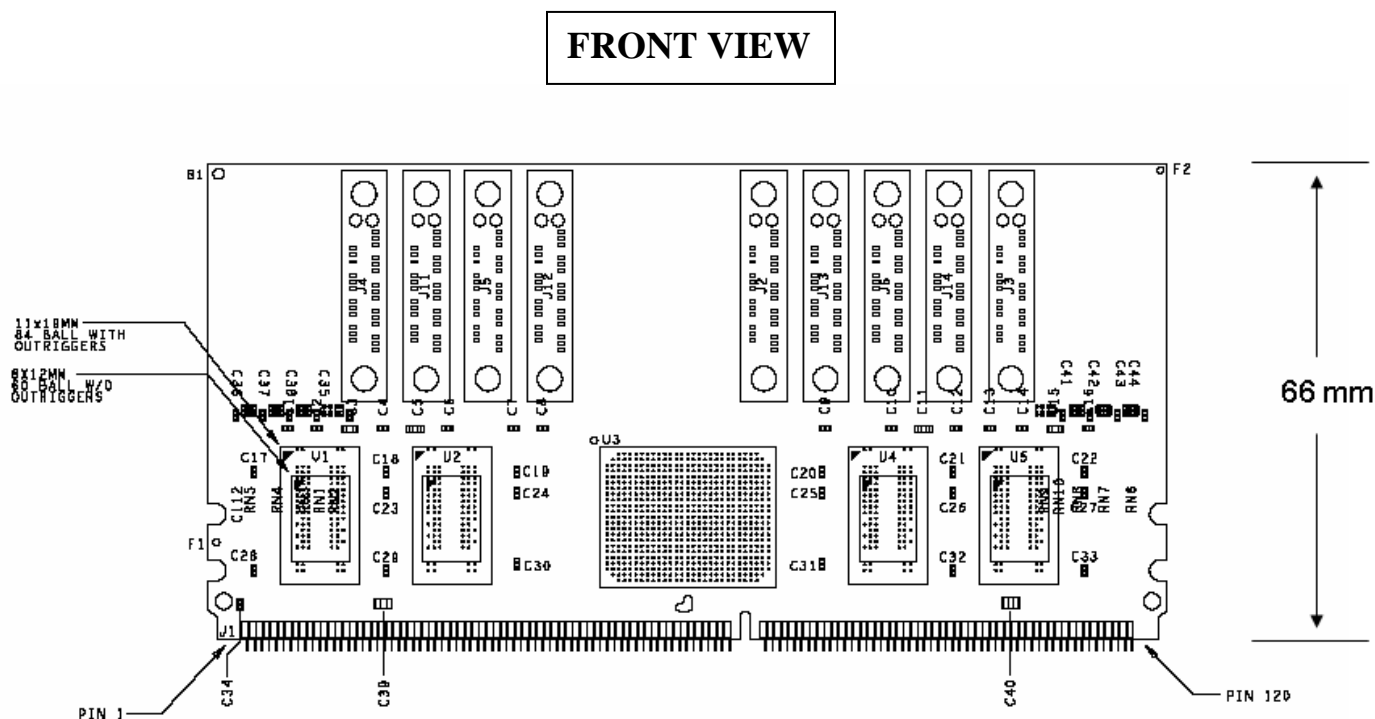
Selective Clocking stores data when commands are present and for 13 clock cycles after Column Address Assertion. This results in fewer Idle cycles being stored in acquisition memory.

Pre-Defined Symbols for easy trigger setup. Available for the following commands: *Read Col Address Read, Write Col Address Write, Mode Register Set, Row Address Strobe, Precharge, No Operation, Ignore Command Data, Burst Stop, Refresh, and Precharge Select Bank.*

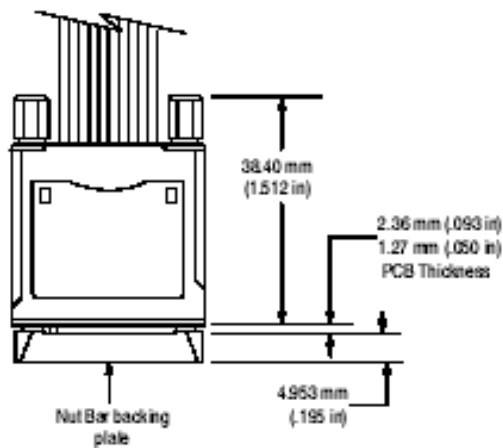
No Dedicated Slot Required – The logic analyzer connects above the normal FB DIMM height so that there is no interference with adjacent DIMMs.

Mechanical Outline

While each NEX-FBDNEXVu667x8DRx/4xSRx DIMM varies slightly, the only variation from a standard DIMM is the height. Approximately 1 3/8" has been added to the height.

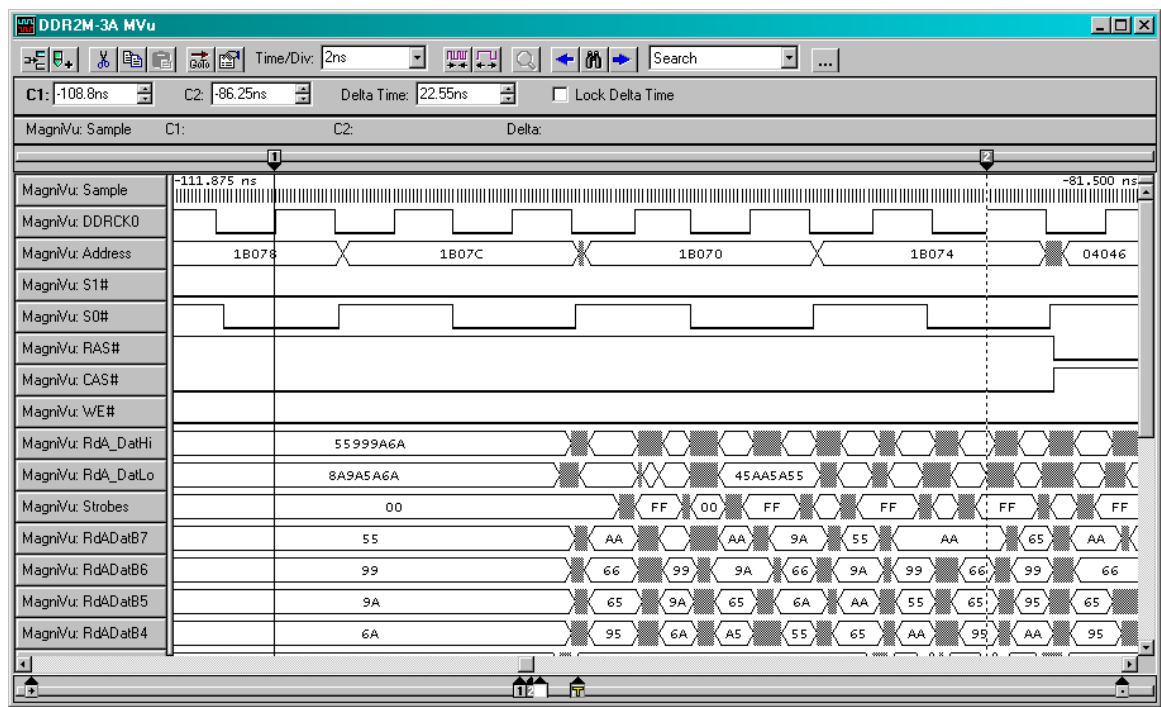


Note: This mechanical drawing of the NEX-FBDNEXVu667x8DRx/4xSRx DIMM does not show the backside probing option that is available on the product



Approximately 1.5” of horizontal keep-out area is required for the probe attachment to the NEX-FBDNEXVu667x8DRx/4xSRx DIMM.

Timing Display



NEX-FBDNEXVu667x8DRx/4xSRx Timing Display

State Display

Sample	DDR2M-3A Address	Cmd	DDR2M-3A Mnemonics	DDR2M-3A DataHi	DDR2M-3A DataLo	DDR2M-3A ChkBits	DDR2M-3A DataMasks	Timestamp
42	04047	1A3	ACTV - ROW ADDRESS STROBE (SO#)					3.750 ns
43	-----	1AC	DESL - IGNORE COMMAND					3.750 ns
44	-----	1AC	DESL - IGNORE COMMAND					3.750 ns
45	-----	1AC	DESL - IGNORE COMMAND					3.750 ns
46	04A18	1A4	WRITE - COL ADDR WRITE (SO#)					3.750 ns
47	-----	1AC	DESL - IGNORE COMMAND					3.750 ns
48	04A1C	1A4	WRITE - COL ADDR WRITE (SO#)					3.750 ns
	-----		WRITE DATA	9A995A6A	8A65A595	40	00	
	-----		WRITE DATA	9A995A6A	8A65A595	40	00	
49	-----	1AA	WRITE DATA	659995AA	8AAA5A55	40	00	3.750 ns
	-----		WRITE DATA	659995AA	8AAA5A55	40	00	
50	-----	1AA	WRITE DATA	5566AA55	45AA5A55	80	00	3.750 ns
	-----		WRITE DATA	5566AA55	45AA5A55	80	00	
51	-----	1AA	WRITE DATA	9A9A6A65	45AA5A55	80	00	3.750 ns
	-----		WRITE DATA	9A9A6A65	45AA5A55	80	00	
52	-----	1AA	DESL - IGNORE COMMAND					3.750 ns
53	-----	1AA	DESL - IGNORE COMMAND					3.750 ns
54	-----	1AA	DESL - IGNORE COMMAND					3.750 ns
55	-----	1AA	DESL - IGNORE COMMAND					3.750 ns
56	-----	1AA	DESL - IGNORE COMMAND					3.750 ns
57	04247	1A2	PRE - PRECHARGE SELECT BANK (SO#)					3.750 ns
58	-----	1AB	DESL - IGNORE COMMAND					3.750 ns
59	-----	1AB	DESL - IGNORE COMMAND					3.750 ns
60	-----	1AB	DESL - IGNORE COMMAND					3.750 ns
61	04247	1A3	ACTV - ROW ADDRESS STROBE (SO#)					3.750 ns
62	-----	1AD	DESL - IGNORE COMMAND					3.750 ns
63	-----	1AD	DESL - IGNORE COMMAND					3.750 ns
64	-----	1AD	DESL - IGNORE COMMAND					3.750 ns
65	1495F	1A5	READ - COL ADDR READ (SO#)					3.750 ns
66	-----	1AD	DESL - IGNORE COMMAND					3.750 ns
67	1495B	1A5	READ - COL ADDR READ (SO#)					3.750 ns
68	-----	1AD	READ DATA	00000180	00000002	00		3.750 ns
	-----		READ DATA	00000180	00000022	00		
69	14950	1A5	READ - COL ADDR READ (SO#)					3.750 ns
	-----		READ DATA	659995AA	45AA5A55	90		
	-----		READ DATA	659995AA	45AA5A55	90		
	-----		READ DATA	55999A6A	4565A595	90		3.750 ns
70	-----	1AD	READ DATA	55999A6A	4565A595	90		

NEX-FBDNEXVu667x8DRx/4xSRx State Display - Software Mode, Address, Data and Command Cycles Only

Tektronix Logic Analyzer Support and Configuration

To acquire both Read AND Write data a TLA700 equipped with three merged 136-channel 450MHz state speed acquisition modules (TLA7AA4 or TLA7AB4 cards) are required. In addition, four P6860 and four P6864 Tektronix probes are required.

To acquire Read OR Write data a TLA700 equipped with two merged 136-channel 450MHz state speed acquisition modules (TLA7AA4 or TLA7AB4 cards) are required. In addition, eight P6860 Tektronix probes are required. This configuration requires Optional software. Order NEX-FBD-NEXVuSWx

Inquire about your specific application, or see Nexus Technology's website at www.nexustechnology.com.

Ordering / Contact Information

Please see the website or contact us for complete solutions.

Part Number NEX-FBDNEXVu667x8DRx/4xSRx (FBD NEXVu DIMMs)

Includes: Disassembly Software (Optional SW available for two module TLA configurations)
Manual

Options include

Option 1 (Socket for AMB installed, AMB mounted on header)

Postal: Nexus Technology, Inc.
78 Northeastern Blvd. #2
Nashua, NH 03062

Telephone: 877-595-8116

Fax: 877-595-8118

Email: support@nexustechology.com
quotes@nexustechology.com
techsupport@nexustechology.com

Website: www.nexustechology.com

Placing an Order

Credit Card orders can be placed directly at 877-595-8116.

Purchase orders can be faxed to 877-595-8118.

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