LP5-A-CDA-441

4x32 LPDDR5(X) BGA Component | Direct Attach | Oscilloscope

Overview

The LP5-A-CDA-441 Direct Attach BGA interposer enables probing of LPDDR5 and LPDDR5X 4x32 components with an oscilloscope.

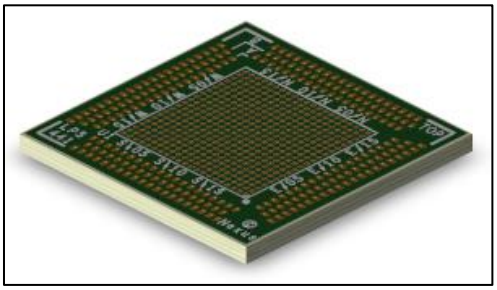


Figure 1 LP5-A-CDA-441 Interposer

- All major oscilloscope vendors supported
- 441-ball 4x32
- LPDDR5X and LPDDR5
- JEDEC Standard JESD209-5
- Easily access signals
- Embedded tap resistors
- Small keep-out volume (KOV)
- Risers available
- S-Parameters for System Simulation
- Oscilloscope de-embedding S-Parameters
- Installs with standard BGA Rework
- Attachment and Analysis Services Available
- Add digital analysis using a PRB-FL probe and a MA51x0 series logic analyzer

XH Series

The LP5-A-CDA-441 is an XH Series interposer, designed to interpose and capture memory signals exceeding 8.5GT/s.

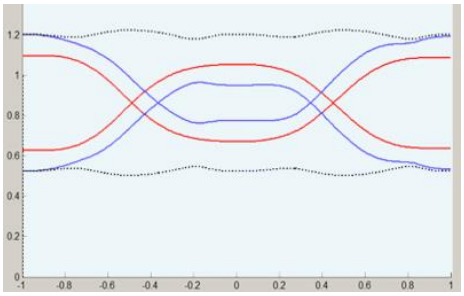


Figure 2 XH Series Interposer Probing

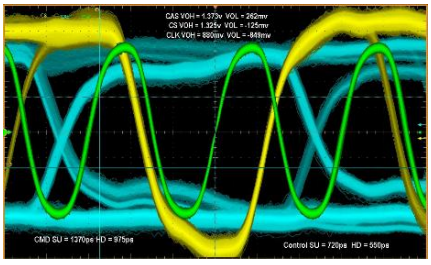


Figure 3 XH Series Interposer Probing

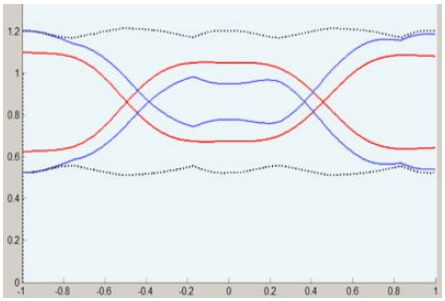


Figure 4 BGA Backside Probing

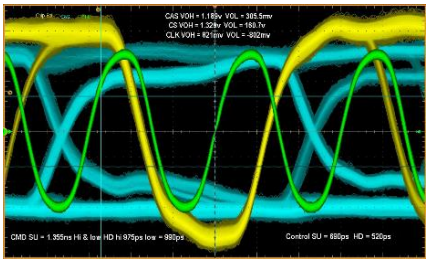


Figure 5 BGA Backside Probing

BGA Interposer Advantages

The LP5-A-CDA-441 interposer enable probing at the highest speeds of LPDDR5X and LPDDR5 with either an oscilloscope or an MA51x0 series analyzer. This enables complete signal access to the DDR5 bus for visibility and compliance analysis. The interposers and risers are easy to install using standard BGA rework practices. Or take advantage of Nexus' attachment and testing services.

Direct Attach – Convenient and Accurate

Optimal LPDDR5(X) validation requires analysis of the LPDDR5 signals as seen by the memory components. This allows for the highest confidence that the signals captured are representative, contain little interference, and present the maximum possible data eye size. This LPDDR5 Direct Attach interposer enables MA51x0 analyzer and oscilloscope probing of the LPDDR5 signals.

Simulation and De-Embedding

S-Parameters are included for target simulation and the creation of oscilloscope de-embedding filters.

Riser

A riser can be used to elevate the interposer over 0.050" (height without including BGA balls). Risers are used to clear components adjacent to the memory BGA. Risers are installed along with the interposer using standard BGA rework practices.

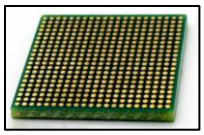


Figure 6 LPDDR5 441 Riser

Attachment and Testing Services

The following services are available for this interposer.

Attachment Service

For each interposer, the *Attachment Service* will install a component to the interposer and the interposer to the target. Other accessories may also be attached (risers, sockets, etc.).

Figure 7 Attachment Service Example

Target Boot & Basic Functionality

For each target, this service will power on and ensure functionality of the target with the interposer(s) installed.

ADD DIGITAL ANALYSIS

Add logic and real-time compliance analysis using a PRB-FL probe and a MA51x0 series logic analyzer.

MA51X0 SERIES ANALYZER & PRB-FL

A MA51x0 series analyzer and a PRB-FL probe enable protocol debug, compliance analysis and oscilloscope cross-triggering. With a turn-key setup, the MA5150 can analyze thousands of real-time memory parameters across clock stops and frequency changes. Also includes 11ps x 10mV x 20-channel analog characterization (iCiS™) and dynamic probe termination.

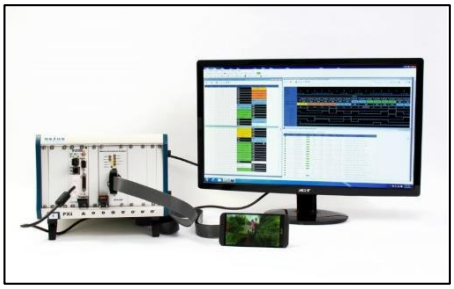


Figure 8 MAx100 Series Analyzer

DIGITAL TESTING SERVICES

MA5150: Signal Analysis & Basic Command Acquisition

This service will power on the target and place the target in a predefined state. A MA5150 analyzer will then be connected to the target and the following tests will be performed and the following reports will be provided.

- iCiS eye analysis report of all command, address and control signals, including recommended sampling positions and a MAx100 System Setup file.
- A real-time JEDEC protocol report, including pass/fail for all basic protocol/sequence checks. Any failures will be noted in the report and an Max100 Saved Session file will be provided so that the customer may review the results.

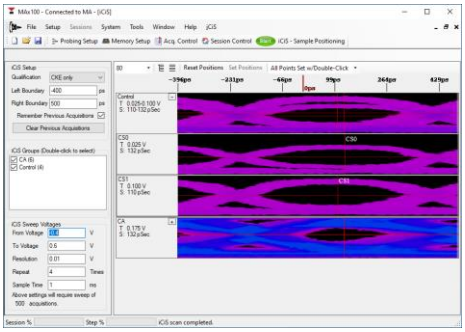


Figure 9 iCiS Analysis Example

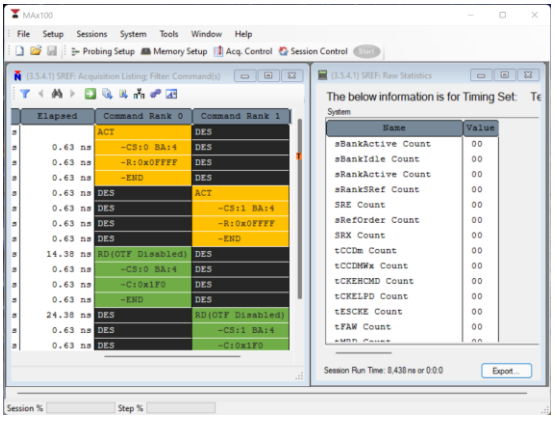


Figure 10 Basic Acq. & Violations Example

MA5150: Margin Testing – One Frequency

This service will power on the target and place the target in a predefined state. A MA5150 analyzer will be used to perform the following tests and the following reports will be provided.

- Real-time MRS/MRW capture of configuration information.
- A real-time JEDEC margin test of one frequency. Any failures will be noted in the report and an Max100 Saved Session file will be provided so that the customer may review the results.

MA5150: Additional / Custom Services

Additional and custom services may also be requested.

DIMENSION DRAWINGS

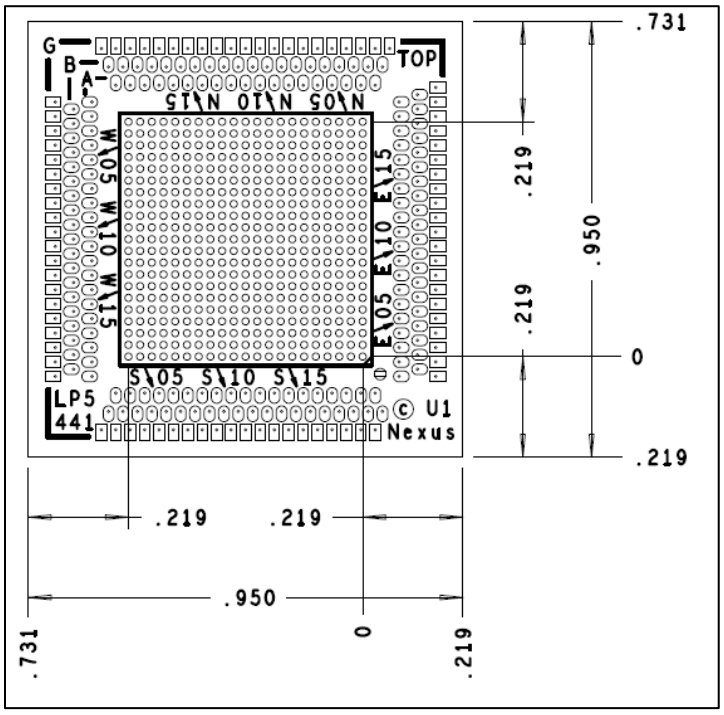


Figure 11 LP5-A-CDA-441 Dimensions - Front

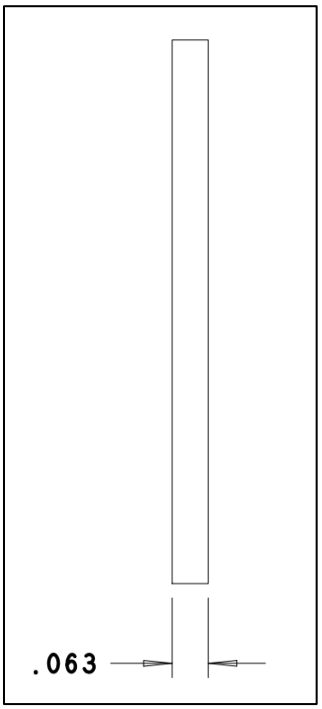


Figure 12 LP5-A-CDA-441 Dimensions - Side

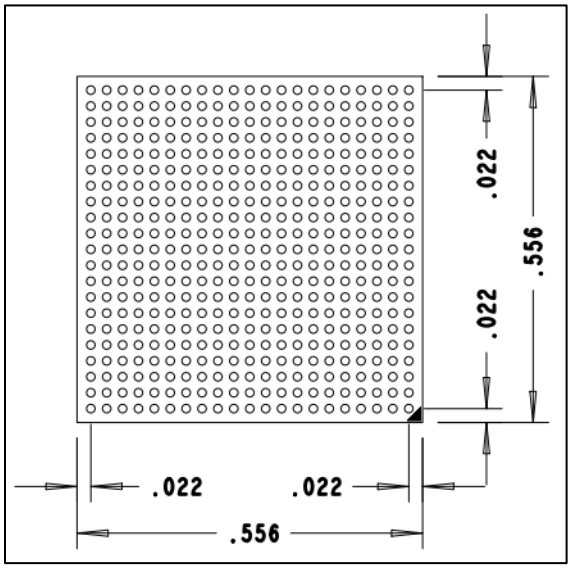


Figure 13 LP5-RSR-441 Dimensions - Front

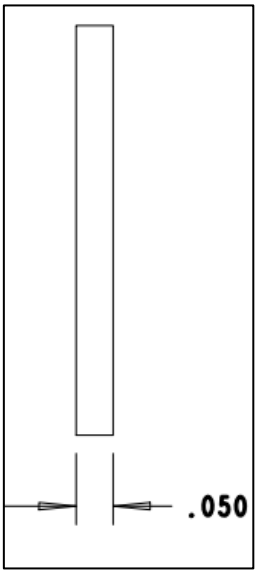


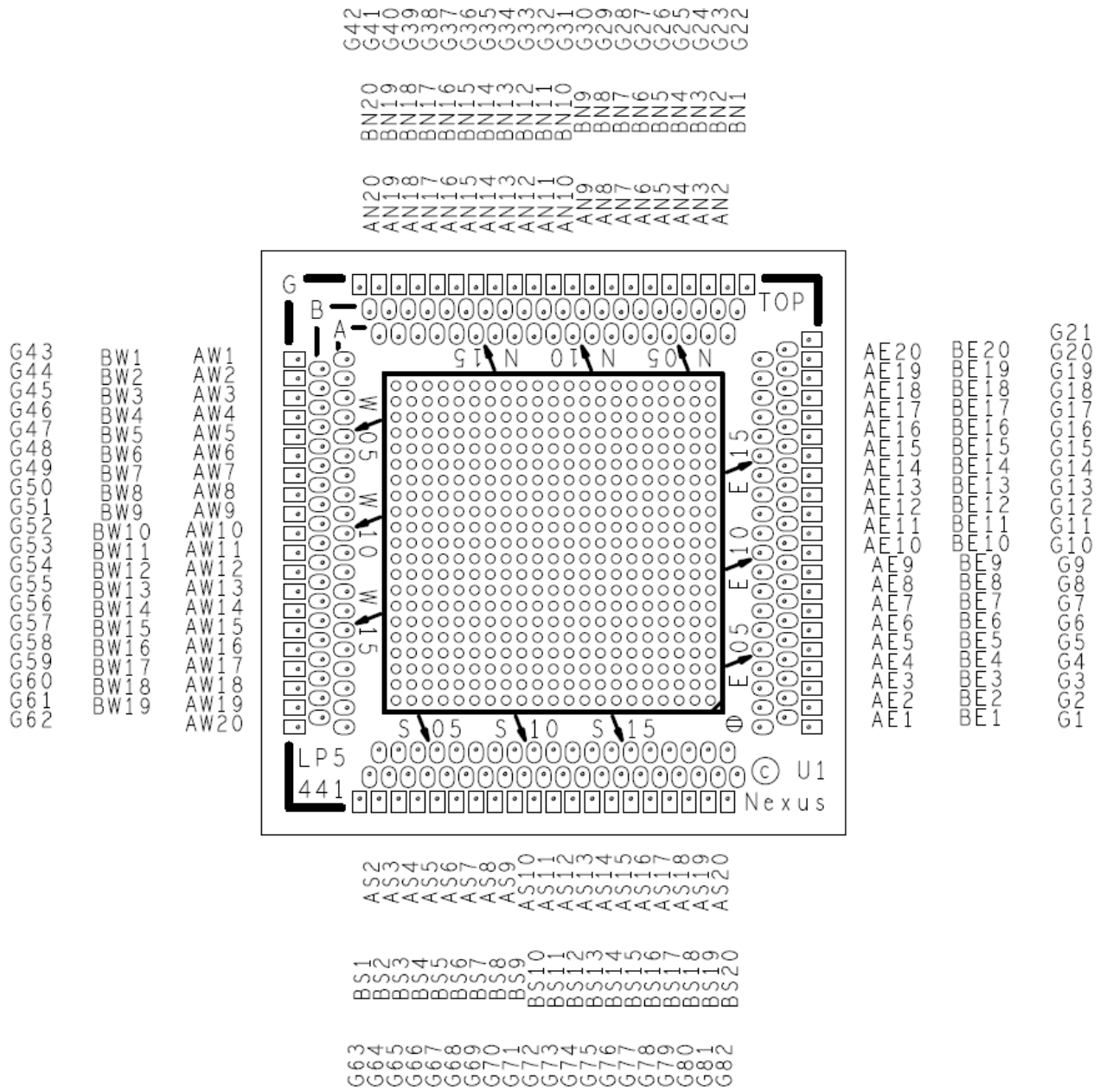
Figure 14 LP5-RSR-441 Dimensions - Side

PROBE POINT SIGNAL LIST

TEST Point	Signal	TEST Point	Signal	TEST Point	Signal	TEST Point	Signal
AE1	WCK0_C_A					AW1	WCK0_C_D
AE2	WCK0_T_A	AN2	DQ9_B	AS2	DQ9_C	AW2	WCK0_T_D
AE3	CA2_A	AN3	CA1_B	AS3	CA1_C	AW3	CA2_D
AE4	DMI0_A	AN4	CA0_B	AS4	CA0_C	AW4	DMI0_D
AE5	DQ4_A	AN5	CS1_B	AS5	CS1_C	AW5	DQ4_D
AE6	RFU1_A	AN6	DQ3_B	AS6	DQ3_C	AW6	RFU1_D
AE7	DQ7_A	AN7	DQ7_B	AS7	DQ7_C	AW7	DQ7_D
AE8	DQ6_A	AN8	DQ2_B	AS8	DQ2_C	AW8	DQ6_D
AE9	CA5_A	AN9	DQ15_D	AS9	DQ15_A	AW9	CA5_D
AE10	CA3_A	AN10	RDQS0_C_B	AS10	RDQS0_C_C	AW10	CA3_D
AE11	DQ6_B	AN11	RDQS0_T_B	AS11	RDQS0_T_C	AW11	DQ6_C
AE12	DQ14_B	AN12	DQ14_D	AS12	DQ14_A	AW12	DQ14_C
AE13	DQ13_B	AN13	DQ8_D	AS13	DQ8_A	AW13	DQ13_C
AE14	DQ12_B	AN14	DMI1_D	AS14	DMI1_A	AW14	DQ12_C
AE15	CA3_B	AN15	DQ10_D	AS15	DQ10_A	AW15	CA3_C
AE16	CA5_B	AN16	DQ11_D	AS16	DQ11_A	AW16	CA5_C
AE17	CA6_B	AN17	CA1_D	AS17	CA1_A	AW17	CA6_C
AE18	DMI1_B	AN18	RDQS1_T_D	AS18	RDQS1_T_A	AW18	DMI1_C
AE19	RFU1_B	AN19	RDQS1_C_D	AS19	RDQS1_C_A	AW19	RFU1_C
AE20	RFU0_B	AN20	DQ0_D	AS20	DQ0_A	AW20	RFU0_C
BE1	DQ1_A	BN1	DQ8_B	BS1	DQ8_C	BW1	DQ1_D
BE2	CS1_A	BN2	DQ10_B	BS2	DQ10_C	BW2	CS1_D
BE3	RDQS0_C_A	BN3	CS0_B	BS3	CS0_C	BW3	RDQS0_C_D
BE4	RDQS0_T_A	BN4	DQ11_B	BS4	DQ11_C	BW4	RDQS0_T_D
BE5	RFU0_A	BN5	DQ5_B	BS5	DQ5_C	BW5	RFU0_D
BE6	DQ5_A	BN6	WCK0_T_B	BS6	WCK0_T_C	BW6	DQ5_D
BE7	CK_T_A	BN7	WCK0_C_B	BS7	WCK0_C_C	BW7	CK_T_D
BE8	CK_C_A	BN8	DMI0_B	BS8	DMI0_C	BW8	CK_C_D
BE9	CA4_A	BN9	DQ0_B	BS9	DQ0_C	BW9	CA4_D
BE10	CA4_B	BN10	DQ1_B	BS10	DQ1_C	BW10	CA4_C
BE11	DQ15_B	BN11	DQ13_D	BS11	DQ13_A	BW11	DQ15_C
BE12	CK_C_B	BN12	WCK1_T_D	BS12	WCK1_T_A	BW12	CK_C_C
BE13	CK_T_B	BN13	WCK1_C_D	BS13	WCK1_C_A	BW13	CK_T_C
BE14	DQ4_B	BN14	DQ9_D	BS14	DQ9_A	BW14	DQ4_C
BE15	RDQS1_C_B	BN15	DQ12_D	BS15	DQ12_A	BW15	RDQS1_C_C
BE16	RDQS1_T_B	BN16	CA6_D	BS16	CA6_A	BW16	RDQS1_T_C
BE17	WCK1_C_B	BN17	CS0_D	BS17	CS0_A	BW17	WCK1_C_C
BE18	WCK1_T_B	BN18	CA0_D	BS18	CA0_A	BW18	WCK1_T_C
BE19	CA2_B	BN19	DQ3_D	BS19	DQ3_A	BW19	CA2_C
BE20	RESET_N	BN20	DQ2_D	BS20	DQ2_A	BW20	

- Test Point G1 Through G82: Signal Ground

PROBE POINT LOCATIONS



PRODUCT CONFIGURATION TABLE

Product Name	Description	Nexus Order Number
LP5-A-CDA-441	LPDDR5 441-ball component interposer for use with oscilloscopes.	NEX-LP5-A-CDA-441
LP5-RSR-441	LPDDR5 441-ball riser. Riser elevated interposer 0.050”	NEX-RSRLPDDR5441[1]

1 P/N NEX-RSRLPDDR5441 includes solderballs.

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