

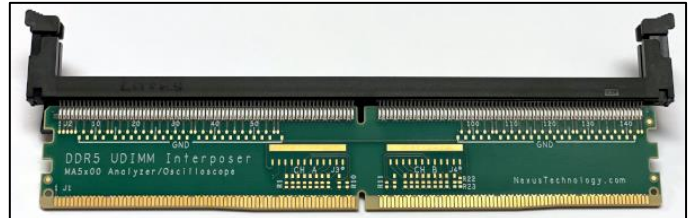
DDR5 Interposers

UDIMM | 288-pin | Oscilloscopes

OVERVIEW

The DDR5-A-UDM-288 unbuffered dual-inline memory module (UDIMM) interposer enables probing of DDR5 UDIMMs with an oscilloscope.

- All major oscilloscope vendors supported
- 288-pin, UDIMM
- JEDEC Standard JESD79-5
- Easily access signals
- Small keep-out volume (KOV)
- S-Parameters for system simulation
- Oscilloscope de-embedding S-Parameters
- Add digital analysis using the DDR5-D-UDM-288 interposer



MIDBUS PROBING

The DDR5-A-UDM-288 is a midbus probing solution. This enables complete signal access to the DDR5 bus for visibility and compliance analysis using a convenient UDIMM slot interposer. XH Series BGA interposers are also available for DDR5.

SIMULATION AND DE-EMBEDDING

S-Parameters are included for target simulation and the creation of oscilloscope de-embedding filters.

SIGNALS PROBED

All signals are probed.

- | | | |
|-----------------------|-------------------------|----------|
| - CK0_A/B | - DQS0_A/B – DQS4_A/B | - RFU3 |
| - CK0#_A/B | - DQS0#_A/B – DQS4#_A/B | - RFU7 |
| - CK1_A/B | - CB0_A/B – CB3_A/B | - RFU143 |
| - CK1#_A/B | - HSCL | - RFU144 |
| - CS0#_A/B – CS1#_A/B | - HSCA | - RFU149 |
| - CA0_A/B – CA12_A/B | - HAS | - RFU152 |
| - ALERT#_A/B | - PWR_GOOD | - RFU213 |
| - RESET#_A/B | - PWR_EN | - RFU226 |
| - DQ0_A/B – DQ31_A/B | - VIN_BULK | - RFU288 |
| - DM0#_A/B – DM3#_A/B | - RFU2 | |

DIMENSION DRAWINGS

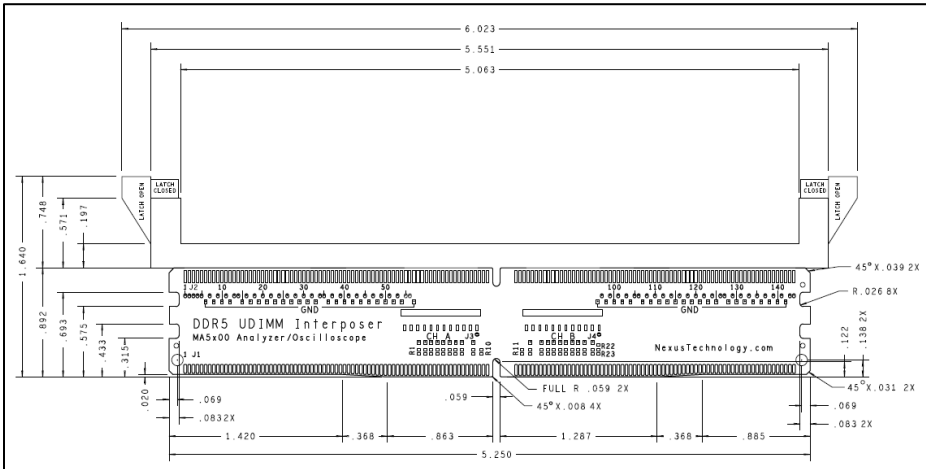


Figure 1 DDR5-A-UDM-288 - Dimensions Front

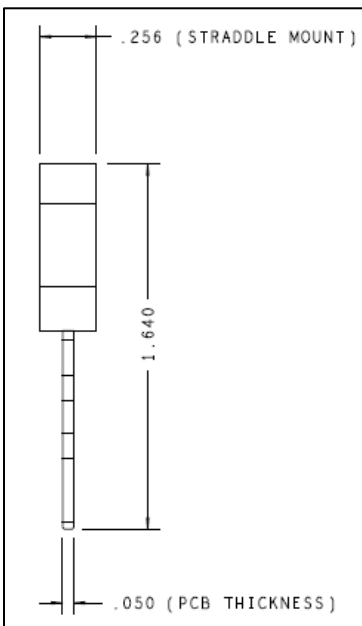


Figure 2 DDR5-A-UDM-288 - Dimensions Side

TESTING SERVICES

The following services are available for this interposer.

TARGET BOOT & BASIC FUNCTIONALITY

For each target, this service will power on and ensure functionality of the target with the interposer(s) installed.

ADD DIGITAL ANALYSIS

Add logic and real-time compliance analysis using a DDR5-D-UDM-288 interposer and a MA51x0 series logic analyzer.

MA51X0 SERIES ANALYZER & DDR5-D-UDM-288

A MA51x0 series analyzer and a DDR5-D-UDM-288 interposer enable protocol debug, compliance analysis and oscilloscope cross-triggering. With a turn-key setup, the MA51x0 can analyze thousands of real-time memory parameters across clock stops and frequency changes. Also includes 11ps x 10mV x 20-channel analog characterization (iCIS™) and dynamic probe termination.



PRODUCT CONFIGURATION TABLE

Product Name	Description	Nexus Order Number
DDR5-A-UDM-288	DDR5 UDIMM Interposer for Oscilloscopes	NEX-DDR5-A-UDM-288



www.nexustechnology.com
support@nexustechnology.com

877-595-8116

603-329-3083 (Outside USA)

78 Northeastern Blvd., Unit 2 Nashua, NH 03062