MA5100 Memory Analyzer

Benchtop Memory Analyzer

- Automated analysis runs for everything from detailed setup information to quick summary runs, to in-depth extended data logging or margin testing runs
- ClockSafe™: Continuous analysis across clock stops and clock frequency changes
- Analog eye characterization at 11ps x 10mV
- Correlate with an oscilloscope for memory DQ data capture
- Integrated Windows 10 Controller

Specifications

- LPDDR5X-9600
- DDR5-4800
- LPDDR4X-4267
- ClockSafe™
- 20 input channels
- 1G-sample acquisition depth
- Programmable probe termination
- 11ps x 10mV x 20-channel analog characterization (iCiS™)
- Real-time smart single frequency or 16 frequency analysis
- Real-time memory performance metrics
- Real-time memory compliance margins and validation
- Trigger in and trigger out

Key Features

- Application software ready for bench, remote-to-lab or offline operation
- Application includes advanced listing, waveform, tables and charting
- Turnkey setup, including automated MRW capture and analysis
- Patented interposer/probe designs
- Analyze thousands of real-time memory parameters
- Full featured, industry standard trigger system

Applications

- DDR5, LPDDR5, LPDDR5x, LPDDR4, LPDDR4x and/or LPDDR3
- Memory validation and debug
- Monitoring bus traffic
- Bus traffic measurement
- Optimization of memory performance
- Analog insight
- JEDEC JESD79-5 rates to DDR5-4800
- JEDEC JESD209-5 rates to LPDDR5X-9600
- JEDEC JESD209-4 rates to LPDDR4X-4267
- JEDEC JESD209-3 rates to LPDDR3-2133

NEXUS TECHNOLOGY

NexusTechnology.com

Results Overview

State Capture

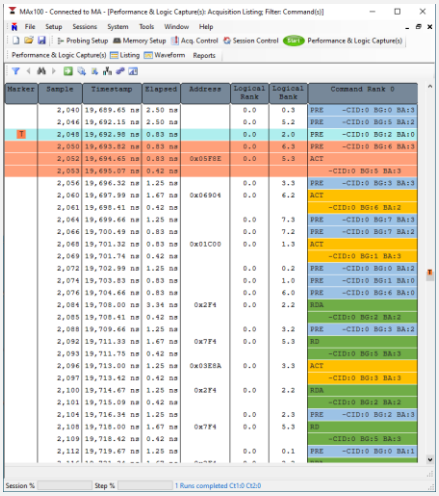


Figure 1 DDR5 State Listing Example

State capture results include continuous traffic around one or more events of interest. The traffic, which may consist of time, bus commands, bus addressing, margin violations, and trigger events, is presented in listing or waveform displays.

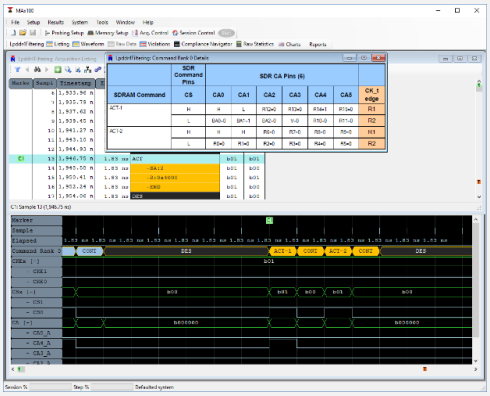


Figure 2 LPDDR4 State, Waveform and Details Example

State capture depths from one hundred samples to one billion samples is available. Advanced acquisition controls monitor and respond to the continuous traffic in real-time to best utilize the state capture memory. Advanced post-capture search and filter can quickly parse the acquisition store.

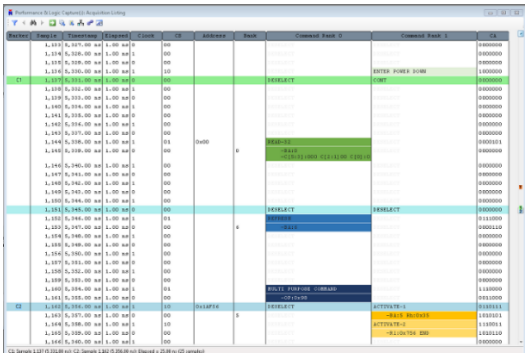


Figure 3 LPDDR5 State Listing Example

Real-time Continuous Analysis

Real-time analysis provides data results during and after analysis runs which may be extremely long (days) or very short (nano-seconds). During the run, analysis is continuous and in real-time. Any event that occurs during the run is captured and analyzed.

Performance

Memory performance metrics include real-time margin metrics and margin violations. For each margin test, results indicate test coverage, observed margin values, as well as flags indicating margin violations. All data is continuously acquired in real-time with results updates continuously while the analyzer is still running. Memory performance metrics also include continuous real-time charting of bus performance characteristics such as throughput, utilization, power management, and more.

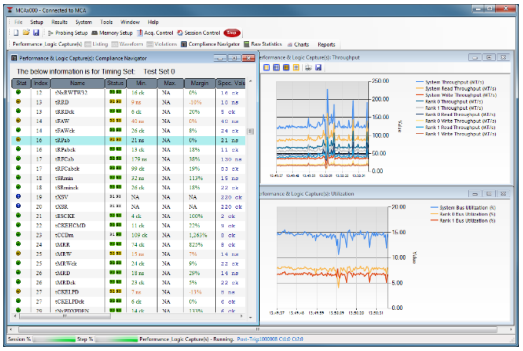


Figure 4 LPDDR4 Real-time / Performance Results Example

True Analog Visibility

iCiS™ provides detailed and invaluable insight of signal quality and expected performance for data acquisition you can trust.

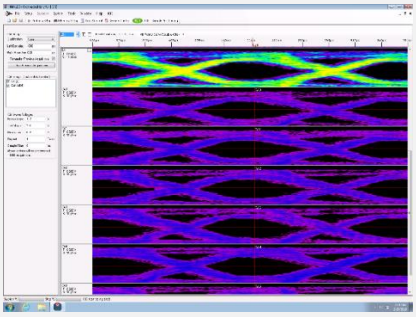


Figure 5 LPDDR4 iCiS™ Example

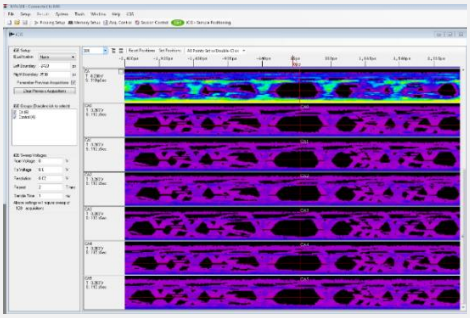


Figure 6 LPDDR4 iCiS™ Example

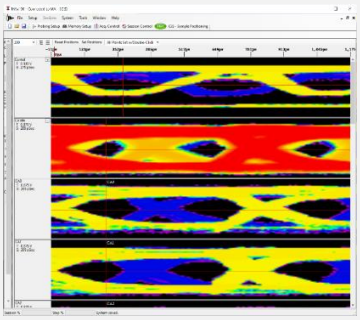


Figure 7 DDR5 iCiS™ Example

Automated Analysis

Analysis is automated and continuous from the time the user clicks the Start button until the analysis session completes. While running, the session updates the application with real-time results.

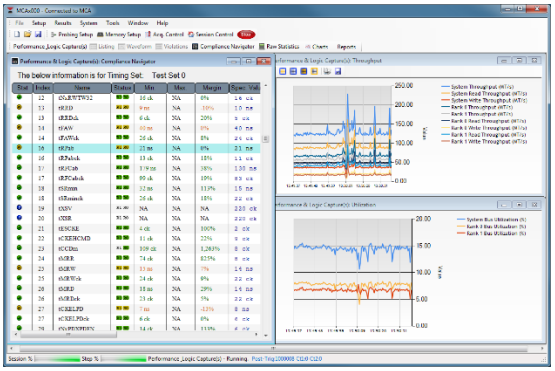


Figure 8 MA5100 Performance Metrics

In the MA5100 Performance Metrics image you can see real-time margins for all compliance parameters as well as a chart of read/write bus throughput.

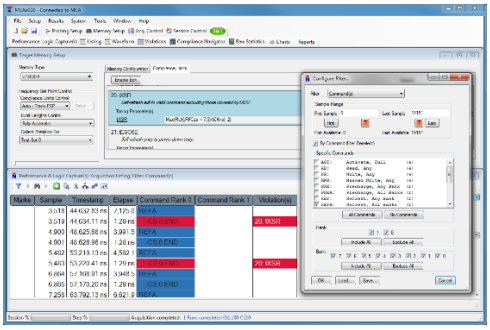


Figure 9 Violation Example

In this example, the analyzer is configured to continuously monitor acquire data until the first occurrence of a compliance violation occurs. That's three simultaneous measurements, each collecting/monitoring real-time data.

ClockSafe™

The memory clock stops and changes frequencies during initialization and calibration. It may also stop and change frequencies during normal operation. ClockSafe™ provides continuous acquisition across these clock stops and frequency changes through a robust acquisition interface that can handle any clock frequency from 0MHz to 2.4GHz. ClockSafe™ also provides continuous analysis by performing real-time measurements in nanoseconds (ns). This is critical for accurate measurements which would otherwise be corrupted when the clock stopped or changed

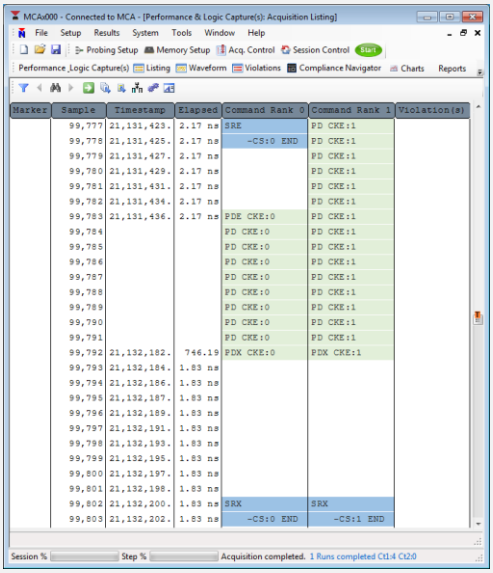


Figure 10 Clock Stop Example

frequencies. Analysis in nanoseconds (ns) is specified for a number of measurements in the JEDEC specifications. ClockSafe™ ensures these measurements are performed, not only correctly, but also accurately.

Smart Sixteen Frequency Analysis

Why analyze one frequency at a time when you can analyze all of them at once?

With aggressively changes frequencies, LPDDR4 presents a challenging analysis environment for most other analyzers but not for the MA5100 with Smart Sixteen Frequency Analysis and ClockSafe™.

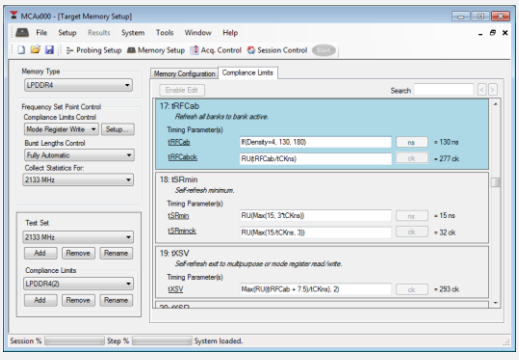


Figure 11 LPDDR5 16-Frequency Setup Example

With the push of a button the MA5100 starts acquiring and analyzing the memory bus in real-time. When a frequency change occurs, the analyzer responds, in real-time, collecting statistics for any one or all frequencies as well as margin testing (looking for violations) specific to each, of up to sixteen, independent frequencies and sixteen sets of margin limits. What does this mean for our users? It means they can run the analyzer once and verify the protocol and margins for every command – missing nothing – in real-time for every frequency.

Reliable Connection

DDR5, LPDDR5(X), LPDDR4(X) and LPDDR3 interposers and probes provide connection between the analyzer and the target while preserving analog signal characteristics.

Attachment Service

DDR5, LPDDR5(X), LPDDR4(X) and LPDDR3 memory components are available in a variety of packages. Many packages are very fine pitch BGA which typically live on densely populated targets. This presents a challenging probing environment and an opportunity to provide our expert services. We provide attachment services for all of our component/package interposers so that our customers are up and running quickly and reliably.

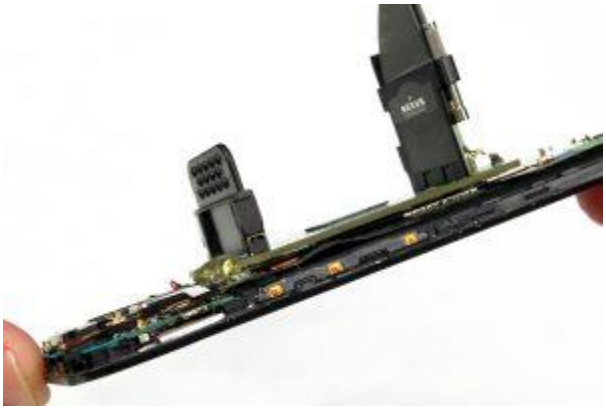
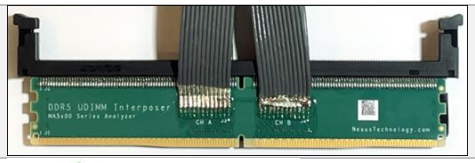
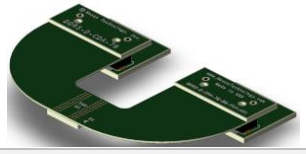
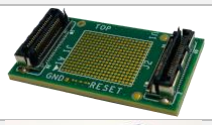
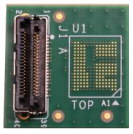
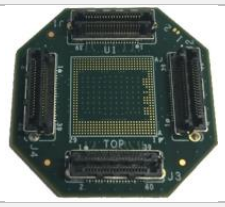
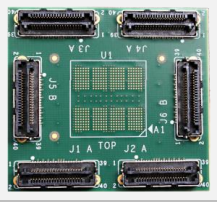
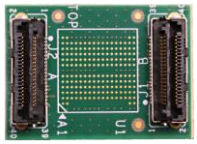


Figure 12 Attachment Service Example

MA5100 Analyzer Interposers

Product Name	Specification	Type	Risers Available	Product Image
DDR5-D-UDM-288	DDR5	UDIMM Slot Interposer	NA	
DDR5-D-CDA-78	DDR5	X4/x8 BGA Interposer	Yes	
DDR5-D-CDA-106	DDR5	x16 BGA Interposer	Yes	*
LP5-D-CDA-315	LPDDR5(X)	2x16 BGA Interposer	Yes	
LP5-D-CDA-496	LPDDR5(X)	4x16 BGA Interposer	Yes	
LP4-D-CDA-149	LPDDR4(X)	2x16 BGA Interposer	Yes	
LP4-D-CDA-200	LPDDR4(X)	2x16 BGA Interposer	Yes	
LP4-D-CDA-254	LPDDR4(X)	2x16 BGA Interposer	Yes	
LP4-D-CDA-272	LPDDR4(X)	4x16 BGA Interposer	Yes	*
LP4-D-CDA-366	LPDDR4(X)	4x16 BGA Interposer	Yes	
LP4-D-CDA-432	LPDDR4(X)	4x16 BGA Interposer	Yes	

LP3-D-CDA-178	LPDDR3	2x32 BGA Interposer	Yes	

*We're always adding more support. Contact us for the latest list of available interposers and information
* Custom interposers are always available

Analyzer Probes

Product Name	DDR Channels Supported	Channels Probed	Connection	DDR5	LPDDR5	DDR4	LPDDR4	DDR3	LPDDR3
PRB-HD-H10	1	1 diff.clock 10 channels	HD, Horiz.	x	x		x		X
PRB-HD-H20	1	1 diff. clock 20 channels	HD, Horiz.	x	x		x		X
PRB-HD-V10	1	1 diff. clock 10 channels	HD, Vert.	x	x		x		X
PRB-FL-20	1 or 2	1 diff. clock 20 channels	Flying-Lead	x	x	x	x	x	X
PRB-P69	1 or 2	1 diff. clock 32 channels	P6900 Midbus	x	x	x	x	x	x
PRB-XL-1	1 or 2	1 diff. clock 33 channels	DIMM / SOIMM	x	x	x	x	x	x

Product Configuration Table

Product Name	Description	Nexus Order Number
MA5100	Benchtop analyzer for DDR5, LPDDR5(X), LPDDR4(X) and LPDDR3.	Contact us for configuration options

SCAN ME

Figure 13 MA5100 Website

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